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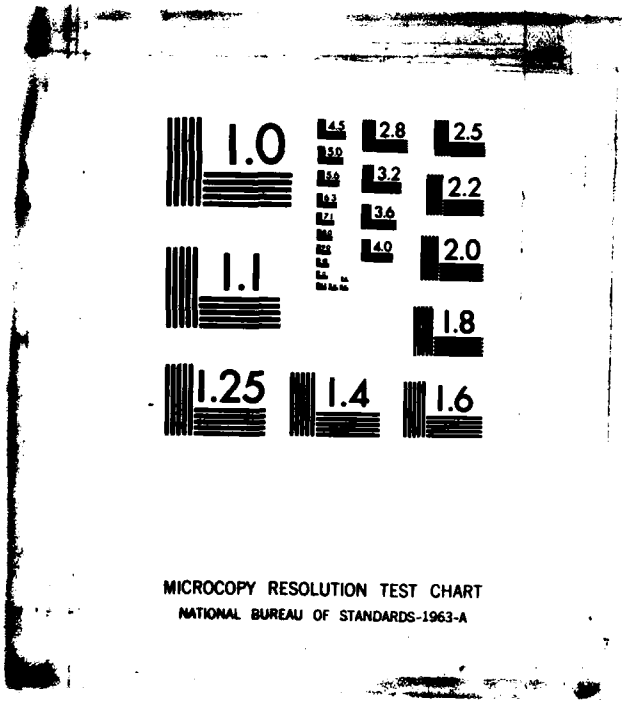
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IMPACT OF ELECTROSTATICS ON IC FABRICATION

Prepared for:

Naval Sea Systems Command
NAVSEA Code 06C31
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Integrated circuit fabrication processes inherently involve materials with a high propensity of triboelectric charge generation. This report details the results of a study in which the intent was 1) to determine how electrostatic charges can catastrophically dame integrated circuits during their fabrication and 2) to investigate the effect these charges have on individual fabrication processes. Possible reliability implications of the presence of electric charges during fabrication are also hypothesized.

An experiment was also carried out to determine the susceptibility of IC's in wafer form. In these tests, devices were stressed at various levels and then electrically tested to determine their functionality. Additionally, the susceptibility modes of devices in wafer form were compared to those in packaged form.

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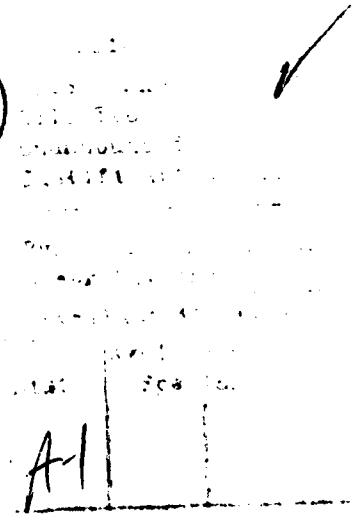
PREFACE

This report was generated as part of the NAVSEA ESD Control Program, Task 3, Contract No. F30602-81-C-0299, Project Plan P-82-006, from funds provided by NAVSEA Code 06C31.



1.0 INTRODUCTION

It is well-known and well-documented that integrated circuits are susceptible to catastrophic damage from electrostatic discharge. This susceptibility to an externally applied voltage transient has been the subject of many studies into areas of device susceptibility modes, susceptibility characteristics, modeling and electrical overstress protection networks. Although this phenomenon has been the subject of much research, perhaps an area of more fundamental importance is the effect unwanted electrostatic charges have on the fabrication process steps and the eventual consequences these effects have on device yield and integrity.

From its infancy, the semiconductor industry has been plagued by so-called random defects. These defects generally appear as missing or unwanted geometries and result in either an initially defective die or possibly as a reliability failure later in the field. Though collectively a very significant failure mode, these defects are very hard to eliminate because they appear to be due to a variety of sources, each individually rare and nearly impossible to reproduce. Advances have been made in this area by increasing clean-room requirements and by new processing techniques. However, these advances have only just kept pace with the increased susceptibility of current technology due to shrinking geometries and expanding die and wafer sizes. Fortunately, recent investigations have uncovered a common thread connecting many of these "random" failure modes. That thread is static electricity.

The intent of this study is twofold: (1) to determine how electrostatic charges can catastrophically destroy ICs during the fabrication process, and (2) to investigate the effects these charges have on the individual processes of device fabrication.

Section 2 of this report will present a discussion of how static is generated with materials normally used in the clean room of an IC fabrication facility and what problems these charges can cause.

Section 3 will discuss how static charges in wafer processing areas can damage ICs on the wafer from electrostatic discharges. It will also present the results of an experiment that was carried out to determine susceptibility levels of devices at the wafer level.

Section 4 will present an overview of each fabrication process and hypothesize possible adverse effects the presence of a static charge can have. The information presentation in this section will be tentative in nature due to the lack of available data on this subjet. Although there was not substantial information available on this subject to draw definitive conclusions, it was the general consensus of industry experts interviewed that there is a definite problem in this area, although many were unable to provide specific instances due to the proprietary nature of these studies at their respective facilites.

2.0 STATIC ELECTRICITY IN A CLEAN ROOM

In an effort to reduce particle-related "random" defects, most wafer fabrication is now performed in clean rooms, typically Class 100 (i.e., a maximum of 100 particles per cubic foot) but as low as Class 10. These clean rooms include filtered air pumped in to provide laminar flow across all work stations, the extensive use of synthetic materials such as polypropalene and nylon, and the requirement that all workers be covered head to toe in synthetic, lint-free smocks. All of these characteristics reduce the risk of particulate contamination, but greatly magnify the risk of static electricity production.

Additionally, many steps in the wafer fabrication process require rather harsh chemicals such as hydrochloric or hydrofloric acid. The prevalence of these corrosive agents has discouraged the use of metals on the wafer fabrication line. Thus, the environment encountered by a wafer in process is composed almost completely of static-generating materials. Further, the requirements for low particle generation also dictate that all surfaces shall be as smooth as possible and cleaned frequently. Again, this is the worst possible situation for prevention of static generation. Generally, the finer the finish on two materials lying against each other the greater the electrostatic charge generated upon separation. In environments which require less-stringent cleanliness, often-handled implements and containers build up a layer of conductive oil from the skin of the workers. This works to suppress static generation. Solder suckers used in electronic board repair are a good example of this effect: while a new one will generate up to 50,000 volts of static electricity when used, a well-used implement will generate less than 1,000 volts. Unfortunately, wafer fabrication areas also prevent this static-limiting effect by frequent cleaning of all work surfaces and implements. Guidelines which minimize operator contact with anything that will contact a wafer also limit this effect. This is done by the use of plastic gloves and tweezers or other detachable handles.

One of the traditional simple cures for static problems is to control the relative humidity of an area to 40% RH or greater. When the relative humidity is high, a thin conductive layer of water will be adsorbed on the surface of most plastics (hygroscopic). This again helps to prevent static generation. Unfortunately, this, too, is prohibited in most wafer processing facilities. Some photoresists are very sensitive to moisture, in that the same thin layer of water which prevents static buildup also affects the adhesion of the photoresist. Thus, areas producing fine-geometry devices generally require a low relative humidity. Additionally, many of the processes in the production of a semiconductor wafer require high-temperature bakes. This tends to dry wafer and carrier surfaces even further. Also, any high-velocity fluid such as deionized water or air (in the case of vacuum pickup) can cause a charge buildup.

Thus, one can easily see that semiconductor fabrication lines have all the conditions necessary for high electrostatic voltage generation. Consider for example, an employee in a nylon coat shuffling across a clean floor in his plastic-soled booties: this employee can easily generate 7,000 to 8,000 volts of static electricity on his body. A fiberglass wafer carrier sliding across a polypropalene tabletop can easily generate 10,000 volts of static. An electrostatic survey of several wafer fabrication lines was recently conducted. This survey used a noncontacting electrostatic voltmeter sensitive to voltages between 500 and 50,000 volts to measure the electrostatic potentials found in these areas. Table 1 lists typical values found on several common articles.

TABLE 1: TYPICAL ELECTROSTATIC VOLTAGES FOUND IN A WAFER FABRICATION AREA

Wafers	5 KV
Wafer Carriers	35 KV
Plexiglas Covers Over Air Bearing Track	8 KV
Tabletop	10 KV

TABLE 1: TYPICAL ELECTROSTATIC VOLTAGES FOUND IN A WAFER FABRICATION AREA (Cont'd)

Storage Cabinet	30 KV
Smocks	10 KV
Quartz Ware	1.5 KV

The areas found to contain the highest electrostatic voltages were those associated with areas which involved high-temperature operations. The high temperatures apparently baked out the moisture layer on these surfaces, thus making them extremely static-generative. Wafer carriers which hold wafers during a dehydration bake are the best example of this effect.

Among the most dangerous areas included in the study were those associated with visual inspections and electrical parameter recordings. These areas combined the worst-case conditions of individual wafer handling, high static charges, and ungrounded conductors in static fields which are brought into close contact with the wafer. Static sparks could actually be observed in some of these areas.

3.0 ESD SUSCEPTIBILITY OF WAFERS

3.1 Introduction

From the preceding discussion one can clearly see that semiconductor wafers are subjected to electrostatic charge throughout the fabrication process. Now consider what effect this charge will have on the wafer. A finished semiconductor, whether bipolar or MOS, is composed of various layers of conductors separated by layers of dielectrics. Generally, the process begins with a substrate of silicon and progresses with dielectric layers of silicon dioxide (SiO_2) and conductive layers of aluminum and/or polysilicon. These processes will be explained in more detail in Section 4. Silicon dioxide has a breakdown voltage of about 10 MV/CM or less depending on the characteristics of the layer. If a 10,000 Å thick layer of SiO_2 were used as a dielectric between conducting layers, a potential of only 1,000 volts would be sufficient to destroy this dielectric. MOS devices or erasable PROMs employing thin oxides of 200 Å - 1,000 Å can expect potentials as low as 30 volts to be destructive.

Consider also the effect the current induced by this electrostatic field may have on a conductive layer in the semiconductor. A worker shuffling across a clean-room floor in his plastic-soled booties may easily develop a 7,000 volt charge. If he now picks up his metal tweezers and grasps a wafer, the charge on his body will be conducted by the sweat layer on his skin through the tweezers to the first conductor encountered on the wafer.

Studies have shown that 100 pF represents a nominal value of capacitance for a human relative to ground and that 1,500 ohms represents a nominal value of contact resistance to a metal conductor. These values are the ones adopted in the military documents on the subject of ESD (Refs. 1 and 2). Now consider the worker who has been charged to 7,000 volts discharging into a device: a theoretical peak current of 4.6 amps would result, sufficient to vaporize small geometry metal or polysilicon lines.

Eukers (Ref. 3) has shown that high-speed spin-drying of wafers can generate 8 KV of static and that when this operation and subsequent tweezer handling were eliminated, 10% fewer deaths resulted compared to a control sample.

Additionally, currents less than that required to open a metal line may also be dangerous. The discharge will probably enter a metal line and then be conducted through a metal-to-diffusion contact to the substrate. If aluminum metallization is used, the short localized high temperature generated by the current spike through the contact may be sufficient to cause rapid alloying of Al into the silicon. This can cause a shorted junction. Worse, it may cause only a leaky junction, which can cause a reliability failure later in life.

The possibilities of latent failures may be of particular concern in devices in which polysilicon gates are utilized. When electrically overstressed they can appear resistive, often making the detection of the fault difficult, hence increasing the possibility of a latent failure.

Packaged semiconductors have been known to be static-sensitive for some time. To prevent damage due to ESD, chip designers generally add input protection to the bond pads on the chip. These input protection networks provide a safe short to the substrate (generally ground) so that the chip will not be damaged by either the high voltage or high currents associated with the discharge (Ref. 4). This technique has proven highly successful for limiting the susceptibility of packaged semiconductors to ESD. But input protection networks provide very little protection for wafers. Speakman (Ref. 5) has shown that the susceptibility of a semiconductor junction is inversely proportional to the area of that junction. Input protection networks are generally designed with larger geometry devices capable of handling much larger amounts of energy than the smaller internal devices on the chip. In a package, electrostatic energy will normally enter the die only through

the wires connecting the bond pads on the chip to the leads on the package. In a wafer, the electrostatic discharge may enter the die at any point on the surface of the wafer. The input protection protects only the bond pads, but the rest of the die is still highly susceptible.

Eukers (Ref. 3) has reported that devices with an ESD immunity of its input protection of 6 KV were being destroyed with tweezer handling after spin-drying of the wafer, indicating that the devices were being destroyed on internal devices since a 6KV ESD immunity level is relatively high.

Contributing to the difficulty in identifying the magnitude of the problem is the fact that a certain number of non-functional die are expected and accepted without failure analysis being performed to verify the cause of failure. There are, however, certain instances where the causes of failure are normally identified. One of these is the situation in which a localized area of the wafer exhibits nonfunctional die. These are considered gross defects which have a "gross yield" associated with them. These gross defects are normally caused by manufacturing errors incurred during the fabrication process such as variations in timing, temperature, and impurity concentrations (Ref. 6), which can result in large variation in device parameters. Another type of defect is called a random defect and includes such defects as random pinholes, random photo defects, and random leakage defects. This type of defect accounts for the majority of device losses and also encompasses the kinds of faults most difficult to identify. Both the devices lost from electrostatic discharges and the ones lost as a result of contamination caused by electrostatic charges would be considered random defects.

Normal good practice in handling wafers is to touch them when necessary on the peripheral of the chip, thus limiting the chance of contamination or degradation (from an ESD) on internal devices. Since many of the devices on the outer edge of the chip are expected to be losses due to geometric considerations, it is an inherently difficult task to prove ESD is a problem affecting wafer yield.

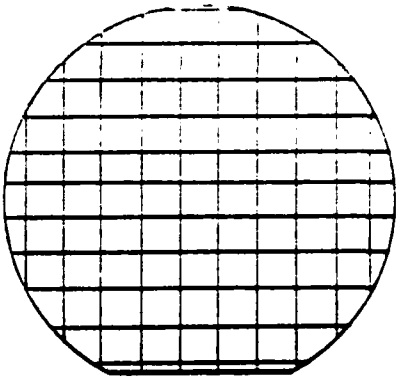
3.2 Wafer ESD Susceptibility Modes

Since it has been shown that there are inherently many triboelectrically "hot" materials used in IC fabrication, it must be understood that a device on the wafer can be destroyed or degraded in various ways. This section will therefore present hypothetical situations which may represent valid susceptibility modes of devices in wafer form. Consider the following: a charged object is brought in the vicinity of a wafer (Figure 3-1). A charge separation takes place on the wafer in line with the orientation of the electric field (E). Now, a reasonably conductive object (a person) contacts one side of the wafer where a net charge is residing (due to the presence of the E field). A grounding takes place, essentially increasing the length of the dipole, causing that net charge to move outward and in turn causing a field-induced electrical transient. It must be noted that when the contact takes place, it does not necessarily have to be a hard ground; that is, an object whose capacitance is sufficient to accept a charge will act as a phantom ground, essentially having the same effect as a hard ground. This situation is analogous to the field-induced discharge model of packaged integrated circuits.

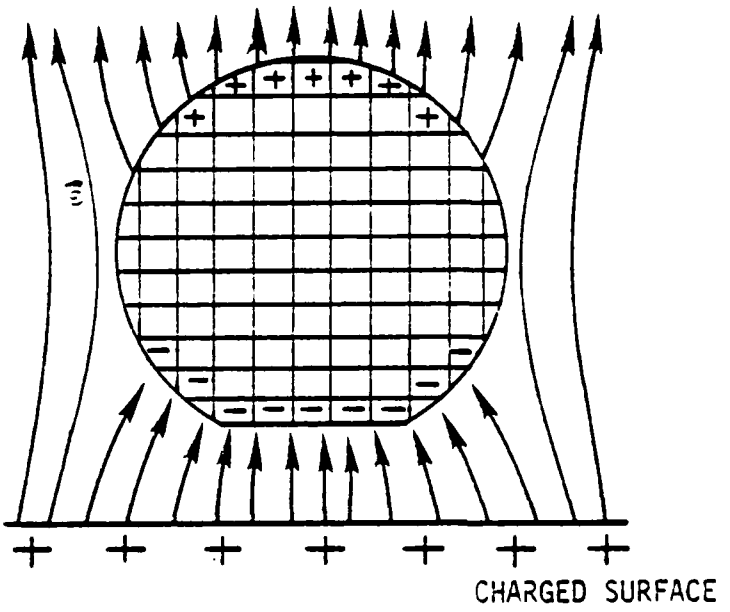
Two more susceptibility modes of devices in wafer form are those by which the wafer capacitance is used to accept or hold a potentially damaging electrostatic charge. The first mode assumes an electrically floating and neutral wafer (Figure 3-2). Next, a charged person or object contacts a random point on the device (on the wafer). The capacitance of the wafer itself (C_1) is acting as a phantom ground in this case, accepting a charge via a current transient through the contact point to the bulk silicon of the wafer. This susceptibility mode is analogous to the floating device model in the case of packaged devices.

The other capacitance-related susceptibility mode is analogous to the charged device model (Ref. 7). It assumes a charge is placed on the wafer (and is stored there via its inherent capacitance to ground).

Electrically Neutral Wafer



Immersing the wafer in an electrical field ($\vec{E}$) from a charged object causing a charge separation.



A point of the wafer is now contacted by a conducting object (grounded or floating) causing a transient current through the point of contact.

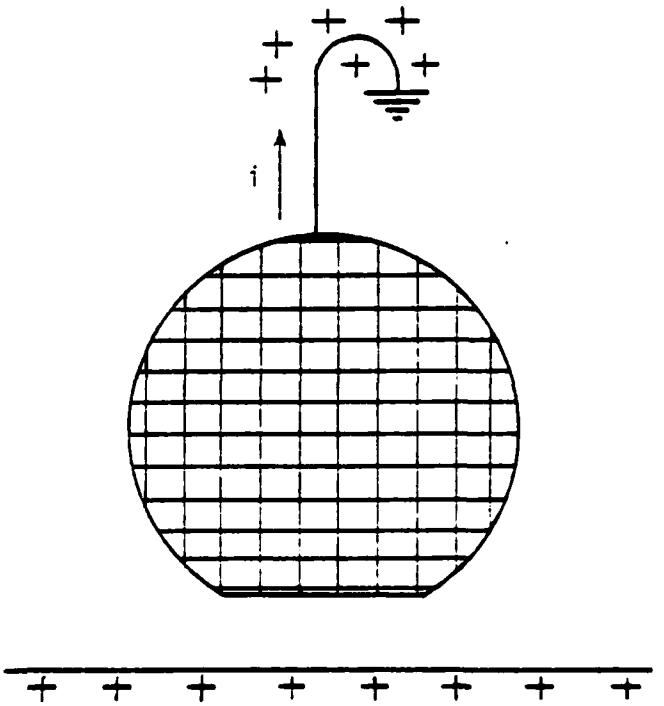
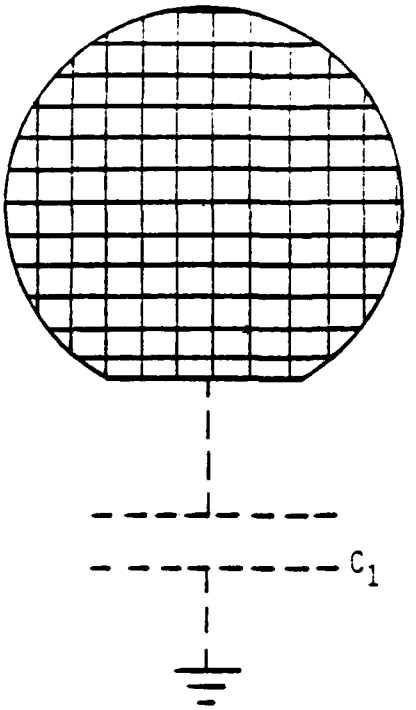


FIGURE 3-1:

Electrically neutral wafer with capacitance (C_1) to ground



A charged object contacts a device on the wafer causing a current transient through the contact point essentially applying a net charge to the capacitance (C_1)

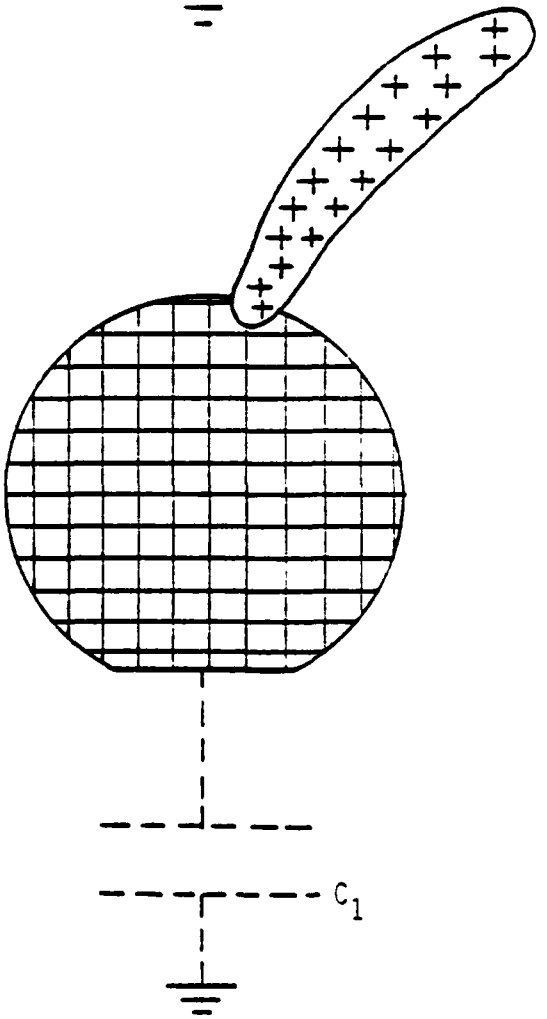


FIGURE 3-2:

Next, a grounded, electrically neutral conductive object is touched to a device on the wafer surface, allowing the charge on the wafer to be grounded and, therefore, causing a current transient.

The charged device model (for packaged devices) assumes a resistance to ground upon contact to be very close to zero. This would indeed also be the worst-case situation for wafers in that it would result in a very high current, short-duration pulse. However, although worst-case, it should be noted that discharges through a higher contact resistance can also result in a failure.

Although capacitance-related failure modes for packaged devices such as the charged device model and the floating device model have been valid susceptibility modes, it is still the human body model discharge which is considered the most prevalent and dangerous situation for ICs. For devices in wafer form, however, this may not aways be true. Since the capacitance-related susceptibility modes are very much dependent on the value of the capacitance (and hence the amount of charge available for discharge), the inherently large capacitance of a wafer (relative to a packaged device) may cause the charged device (or wafer) discharge and the floating device (or wafer) discharge to be the more prevalent susceptibility modes.

It has been shown by Unger et al. (Ref. 7) that the capacitance of a 40-pin DIP lying flat on its back on a ground plane has 52 pF. This capacitance is dependent on the size of the conductive portion of the chip and its relative orientation to ground. Since a wafer's conductive portion is many times larger than that of an individually packaged device, the capacitance will be many times larger. Thus, much more charge is available to be passed through the particular site of the die which is contacted.

3.3 Results of Wafer ESD Tests

In order to test the electrostatic sensitivity of semiconductor wafers, a simulated "zapper" was built. This "zapper" is shown schematically in Figure 3-3. The "zapper" essentially followed the standard human body model. A 100 pF capacitor with one lead grounded is tied through a 1.5K ohm resistor to a brass ball of approximately 5/16" diameter. The ball is first touched to a high-voltage source. This charges the 100 pF capacitor. When the ball is then subsequently touched to a device on the wafer, the 100 pF capacitor is discharged through the 1.5K ohm resistor into the grounded wafer.

To perform the test, a number of MOS semiconductor wafers were obtained and tested using a wafer probe machine. Both functional and parametric tests were performed. Failing die were marked with a red ink dot.

Subsequently, one wafer was set aside as a control, and four other wafers were submitted to a series of simulated zaps. To further insure the cause-and-effect relationship between the zap and any failures, all the good die in every third row were zapped at one of the following voltages: 500, 1000, 2000, or 5000 volts. The wafers were then reprobed. Die failing this time were marked with a green ink dot. The results of this study are shown in Table 2.

TABLE 2: RESULTS OF SIMULATED WAFER ZAP

Simulated Zap Level	Number of Failing Die Pre-Zap	Number of Failing Die Post-Zap	% of Zapped Which Failed
Control	152	154	---
500V	182	218	41%
1 KV	153	222	71%
2 KV	162	214	56%
5 KV	210	250	51%

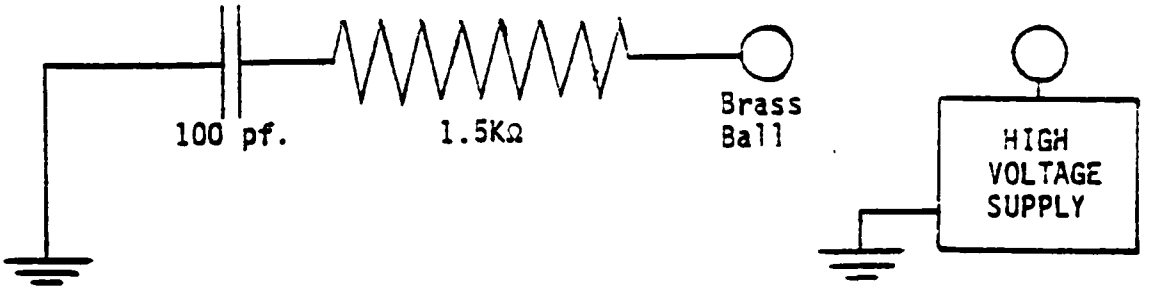


FIGURE 3-3: SIMULATED ZAP CIRCUIT

Even more revealing than the summarized data is the pattern of the zapped wafers on the die. Figure 3-4 illustrates the results of the 1000-volt wafer and clearly shows that the failures did indeed lie in every third row.

To further study this phenomenon, a number of initially good die which failed following a simulated zap were assembled into packages and electrically characterized. The point of failure was then located and photographed. Most of the failures appeared as open metal lines as shown in Figures 3-5 and 3-6. However, poly-metal shorts (Figure 3-7) and thin oxide failures (Figure 3-8) were also identified.

Once it was proven that the die were susceptible to electrostatic voltage as low as 500 volts and that electrostatic potentials above 20,000 volts were available in the clean rooms, it was a simple task to verify the logical conclusion. A number of standard die found to be defective at wafer probe were assembled into packages. Again, these parts were electrically characterized. Those with electrical failure modes similar to those identified in the simulated zap study were analyzed to identify the exact point of failure. The failures are again photographed using a scanning electron microscope (SEM). These photographs were then compared to the failures found during the simulated zap study. Not surprisingly, a number of very similar defects were found (Figure 3-9). Thus, it can be concluded that electrostatic discharge does affect the yield of semiconductor wafers.

All of the wafers studied in this investigation were complete, including a 10,000Å - 15,000Å coating of glass over all of the die except the bond pads. None of the damage identified in the study was associated with the bond pads; thus, a breakdown of the top glass layer must have accompanied the zap.

Please note that the failure modes encountered in this study were related to the materials and geometries used in the semiconductor and

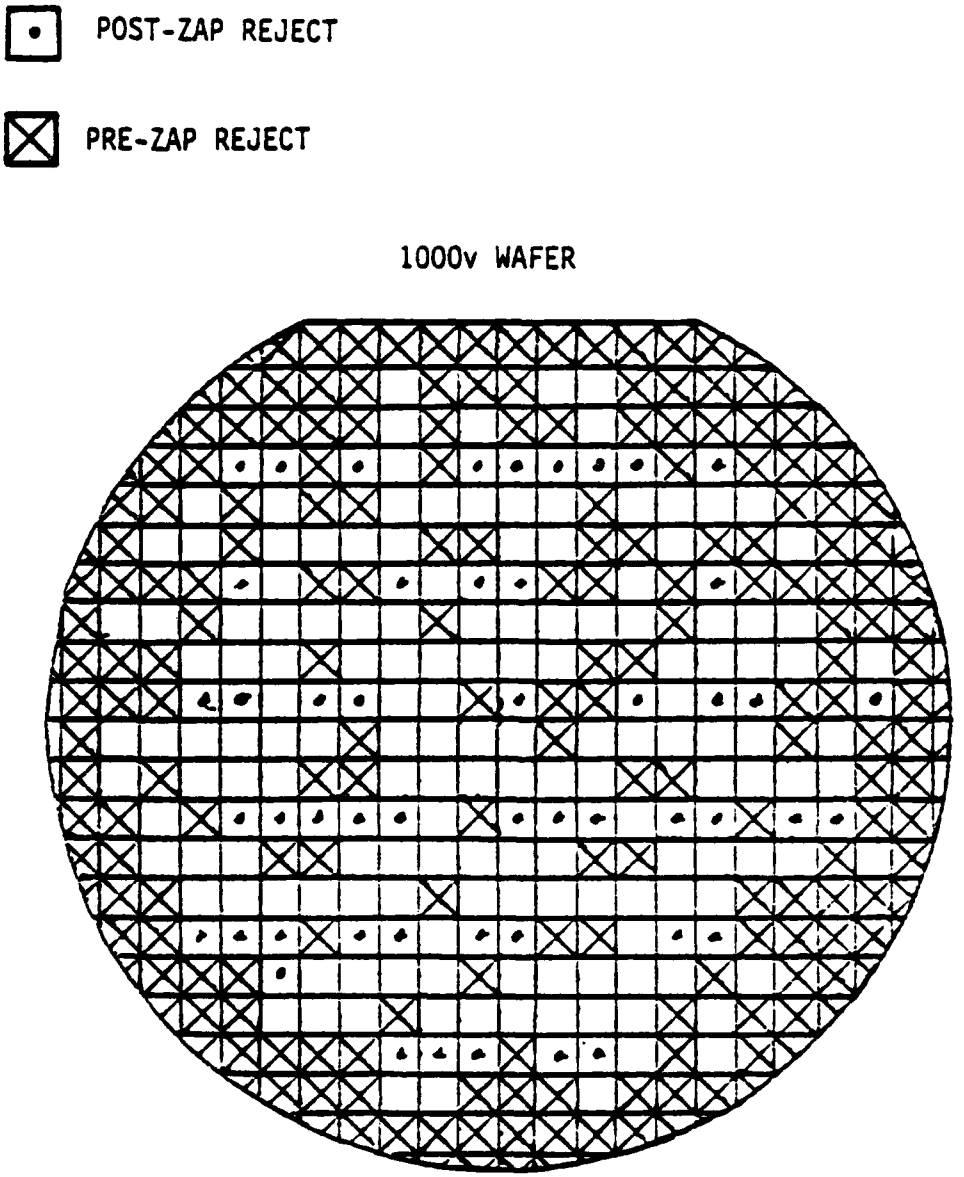


FIGURE 3-4: POST-ZAP FAILURE PATTERN

EVERY GOOD DIE IN EVERY THIRD ROW WAS GIVEN A SIMULATED ZAP

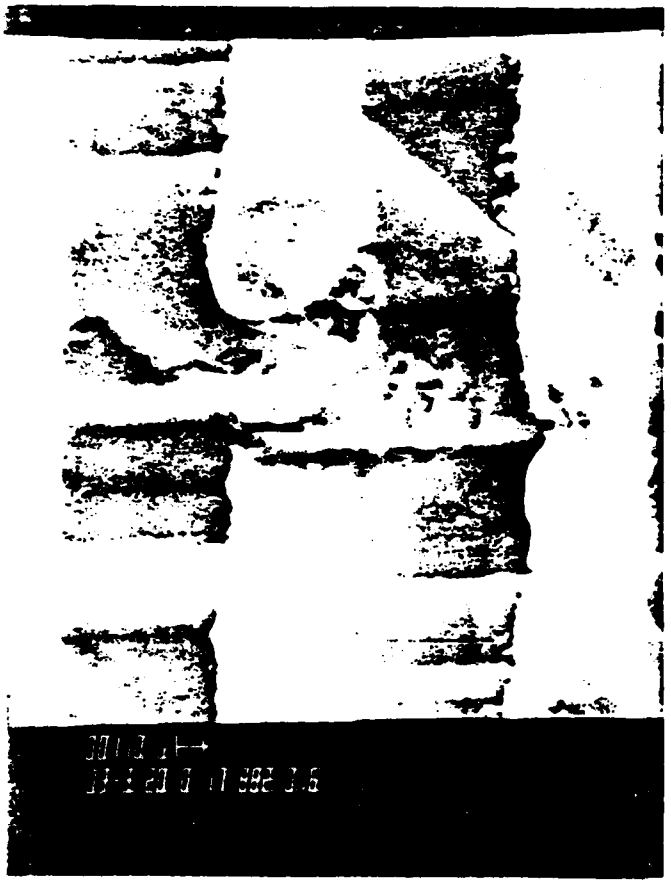


FIGURE 3-5: METAL LINE OPENED BY A SIMULATED ZAP

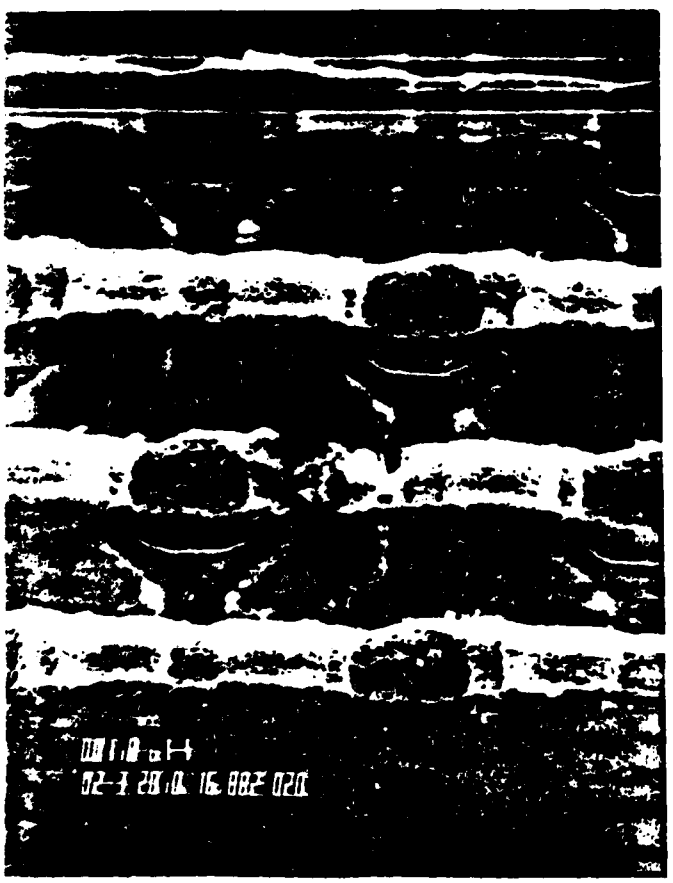


FIGURE 3-6: METAL LINE OPENED BY A SIMULATED ZAP

FIGURE 3-7: POLYSILICON TO METAL SHORT CAUSED BY A SIMULATED ZAP

FIGURE 3-8: THIN OXIDE FAILURE CAUSED BY A SIMULATED ZAP

FIGURE 3-9: METAL TO POLYSILICON SHORT CAUSED BY A LOW CAPACITANCE ZAP

FIGURE 3-10: OPEN METAL LINE CAUSED BY A PARTICLE

were not a function of circuit design or technology. Thus, bipolar devices should be expected to be as susceptible as MOS devices.

3.4 The Effect of ESD on Separated Die

After semiconductor wafers are completed, they are divided into many individual chips and assembled into packages. One may expect separated, individual die to be just as susceptible to ESD as wafers are. This, however, is not true. Individual die subjected to the same human body discharge previously discussed in relation to simulated zaps on wafers could not produce failures below 5,000 volts. This apparent discontinuity can be explained by considering the capacitance of the separated die. The capacitance of a single chip will be less than the 100 pF of discharging capacitance. Thus, only a small portion of the energy stored in the 100 pF capacitor would be transferred to the die. Apparently, this energy was below the damage threshold of the chip at voltages below 5,000 volts. To check this theory, separated die were placed on grounded metal plates and again subjected to simulated human body discharges. This time, failures were found in the die subjected to 500 and 1,000 volt zaps. However, at potentials above 5,000 volts, it was found that the electric field around the base on the simulated zapper was sufficient to actually lift the die from the metal plates before the discharge occurred. Thus, the die was zapped in the air and fell back to the pad. These die were less likely to fail than die zapped at lower voltages on the plates.

3.5 The Effect of ESD on Semiconductor Masks

Patterns used on semiconductor wafers are currently defined using photolithography. The patterns are originally outlined on a set of masks which are laid or projected onto the wafer. The masks are generally composed of a layer of chrome on a glass slide. This presents the same situation as was previously noted on the wafer. Any geometric pattern on the mask will have a finite capacitance. Naturally larger geometries, especially those connected to scribe line delimiters or to the border representing the degree of the mask, will have more

capacitance. The capacitance is a measure of the amount of energy that can be absorbed through a zap of a given voltage. A high capacitance line brought into close proximity with a charged object can pull enough current to vaporize a small amount of chrome. This will cause a defect which will be repeated on each successive wafer exposed using this mask.

Experiments, again using the human body model, have shown that masks can be damaged by electrostatic discharges of 3,000 volts or more.

Please note that the capacitance of any geometry on a mask will be greatly dependent on the alignment of the mask with respect to ground. While the substrate of a wafer can act as a ground plane for higher-layer geometries on the wafer, a mask has no such built-in ground.

Electrostatic damage to a mask is much less likely than electrostatic damage to a wafer in a typical application. This is because only a small percentage of geometries on the mask will have enough capacitance to draw the current necessary to cause the metal to vaporize. Alternately, almost the entire surface of a wafer can be considered static-susceptible. However, a zap to a wafer creates only one defective die. A zap to a mask creates a defective die every time it is used.

3.6 Simulation of Wafer ESD

As we have seen, the sources of static charges are many and varied in a wafer fabrication area; thus, the damage caused by discharges from any of these sources may be considerably different. The human body model (100 pF capacitance and 1.5K ohm resistance) is a good first estimate of an electrostatic discharge model. However, variations in the capacitance, resistance and voltage parameters may make significant differences in the appearance of ESD damage. The studies of wafer zaps described earlier were performed using the human body model. The predominant failure mode found in this study was metal line vaporization. Subsequent studies were performed varying capacitance and resistance. In general, as the capacitance was reduced, the tendency

shifted from vaporized metal to oxide defects. One such example is shown in Figure 3-9. This figure shows only slight metal damage but a clear hole in the oxide. This discharge used a 26 pF capacitor and a 1K ohm resistor. The electrical failure mode was a short between the metal line and the underlying polysilicon.

As the capacitance was further reduced, the voltage required to cause damage increased. Again, oxide breakdown, both thin field and interlevel dielectric, was the prevalent failure mode with low capacitance and high voltage. Alternately, as the resistance was decreased and the capacitance increased, vaporized metal and fused polysilicon resulted. Oxide damage around the vaporized metal was also noted with the larger capacitance. Smith (Ref. 8) has also shown the dependence of pulse width (a function of the source R and C) on the appearance of the failure site.

Masking defects caused by particles on a mask or wafer or in photoresist may cause damage which looks nearly the same as that caused by ESD. However, these defects can only affect one level in any location. ESD usually shows very localized damage to several levels. An example of this can be seen by comparing Figures 3-5 and 3-10. Figure 3-5 shows an open metal line caused by ESD while Figure 3-10 is an open metal line caused by a particle in the photoresist. Note the damage to the underlying oxide in Figure 3-5. Also note the damage to the edge of the adjacent metal line in Figure 3-10, probably caused by the same particle.

4.0 EFFECTS OF ELECTROSTATIC CHARGES ON IC FABRICATION PROCESSES

4.1 Review of Basic Fabrication Processes

In this section, we will present a brief overview of the steps involved in IC fabrication and attempt to identify areas where a static charge could cause adverse effects. All integrated circuits, bipolar and MOS, use the same basic processes in their fabrication. These steps that will be discussed are:

- o Wafer Preparation
- o Epitaxial Growth
- o Photolithography
- o Oxidation
- o Diffusion/Ion Implantation
- o Metallization

Subsequent processing steps such as packaging are beyond the scope of this study and will not be addressed.

Wafer Preparation

The first step in preparing a wafer is growing a silicon ingot. An ingot is grown by controlled cooling of molten silicon around a seed crystal. From this ingot, the actual wafers are obtained by slicing the ingot into thicknesses of approximately 20 to 30 mils. This slicing is accomplished through mechanical sawing.

The next step is to lap and polish the silicon slices which have just been cut to remove the saw marks and to obtain a smooth, essentially flawless surface to accommodate the fabrication of small geometry devices.

Epitaxial Growth

The next step in wafer fabrication is epitaxial layer growth, in which doped silicon is grown on the silicon substrate to form a material from which junctions can be grown. This step is essential for bipolar devices. The silicon for the epitaxial layer is supplied by silicon tetrachloride ($SiCl_4$) or silane (SiH_4) which is heated to produce a high-temperature gas flow ($\approx 1200^{o}C$). At the same time, doping of the epitaxial layer is accomplished by introduction of a P or N type dopant material. The dopant material is either from Group III for P type doping or Group V for N type doping since semiconductor starting materials are from Group IV on the periodic table of elements. The epitaxial growth of the doped silicon drastically reduces the volume resistivity of the surface material to $\approx .1$ - 10 ohm-centimeters.

Photolithography

Photolithographic processes are used to define precise patterns on a wafer such that diffusions or metallization runs can be accomplished as desired. For diffusion processes, the first step is to grow a layer of oxide over the entire surface of the silicon. Next, a film of photosensitive laquer called photoresist is applied to a spinning wafer to allow uniform coverage. Then a mask of the desired geometries is placed on the wafer, which is then exposed to light. The unwanted oxide is then etched away to the silicon surface on which diffusions can now take place. Oxide is used in this process since it acts as a very good barrier to diffusants.

A similar process is followed in defining the metallization runs. The wafer is first coated uniformally with a high-conductivity metal, usually aluminum. Again the photoresist is applied, exposed through a mask, and etched, leaving metal runs in the desired locations. We will explore the effects of static during this process later.

Oxidation

Oxidation is the process by which a layer of silicon dioxide is formed on the surface of a wafer. It is a form of glass and hence has a very high electrical resistivity. It is a critical fabrication process which has been the topic of much investigation.

Oxidation serves a two-fold purpose: to create insulative regions separating various active regions and to form a layer by which photoresist can be applied, exposed and etched to protect and expose desired locations. Silicon dioxide is a very useful microcircuit fabrication material because (1) it has the ability to mask out the most commonly used diffusants, (2) it can be readily etched with high resolution, and (3) it provides good dielectric properties.

Silica glass has an amorphous structure, i.e., it lacks a crystalline form and consists of a random network of silicon and oxygen atoms. Although there are many methods of oxidation (i.e., anodic oxidation, gaseous oxidation, steam oxidation, etc.) they are all a form of "controlled rusting." Normally, oxidation is accomplished by passing oxygen over the surface of the wafer in a furnace heated from 900°C to 1300°C. The rate of growth of the oxide layer is dependent on such factors as time, temperature and pressure.

The effects of the presence of static charge will be discussed further in Section 4.2.2

Diffusion/Ion Implantation

The process of diffusion in the manufacturing sequence is meant to introduce N or P type impurities into exposed regions of the wafer (following a photolithographic process), forming P-N junctions. In this process, a dopant is carried over the silicon wafer at high temperatures within a carrier gas. Some of the variables determining junction characteristics are time and temperature of diffusion, amount and purity of dopants introduced in the gas flow, and cleanliness of the process.

Ion implantation can also be used to form P-N junctions. Here, impurities are introduced into the silicon crystal wafer by subjecting it to a high-energy ion beam. This ion beam is generated by stripping the dopant atoms of one or more electrons and accelerating them through a high potential difference to the silicon wafer surface. The dopant can be selectively deposited by the use of a patterned oxide layer or a photoresist pattern.

Metallization

Metallization is the process by which metal is deposited on the wafer in desired locations to form connecting runs. First, a layer of metal is deposited over the entire surface of the wafer. Next, photoresist is applied, masked, exposed and etched.

4.2 Implications of the Presence of an Electrostatic Charge

Since many of the fabrication processes use energetic beams or particles, an actual charge on or near the wafer is not believed to cause anomalous effects during processing, although there is lack of any definitive data in this area and it should be researched further.

In this study, the main problem areas identified from a charge on or near a wafer are the electrostatic attraction of unwanted stray particles and their eventual effects on device functionality and integrity.

4.2.1 Particulate Contamination

Particles can be filtered out of the air quite effectively; however, this does not eliminate them from the environment of the semiconductor wafer. Particles are also generated at nearly every stage of fabrication. People are probably the biggest source: lint from clothing, hair or dead skin flakes. Broken wafers are another source.

Anytime one surface is scraped against another, some particles may be generated. Quartz wafer boats sliding into quartz tubes, wafers transferred from one carrier to another or plastic boxes opening or closing all may produce particles. Even the air filters themselves may shed fibers.

Thus, particles cannot be totally eliminated from the wafer fabrication process. There is, however, one particle-related effect which is often ignored. Most airborne particles are electrostatically charged. This charge may be generated when the particle is originally scraped off its parent material, or it may pick up a charge as it is blown across a surface.

Since the particle is mobile while floating in the air and highly charged, it will now react to any electrostatic field it finds itself in. Any statically charged surface can provide this field. The higher the electrostatic voltage the stronger the field. Charged particles will be repelled by a similarly charged surface but attracted by an oppositely charged surface. If either the particle or the surface is an insulator, the particle will not be neutralized upon collision and will thus stick to the surface.

Either a wafer or a mask may act as such a charged surface. Since most particles found in semiconductor fabrication areas are nonconductors and large areas of a semiconductor's surface are covered by an oxide during most of the fabrication steps, particles attracted by the electrostatic field of a charged wafer or mask tend to become attached. This electrostatic force of attraction is considerable compared to the force which may be applied to these tiny particles by a stream of compressed air or nitrogen. Even deionized water may not remove some of these particles. Normal tap water would be conductive enough to neutralize the static charge. However, deionized water is an insulator.

4.2.2 Critical Fabrication Processes

The processes identified in this study that are particularly affected by statically induced contaminants are photolithography, epitaxial growth and oxidation. Therefore, these processes will be explored further.

The photolithography process used to produce semiconductors is inherently particle-sensitive. A particle on either the wafer or the mask during the exposure step on any level can cause a defect in the pattern. Depending on the size and location of the particle, this can cause either an initially defective die or a reliability failure later in the life of the part. To prevent particles, Class 100 or Class 10 clean rooms have been developed. However, as geometries shrink, the size of the particles which must be controlled also decreases. Additionally, consider the effect of 30 particles on the surface of a wafer which has 600 die per wafer, compared to the effect of these same 30 particles on a wafer which has only 300 larger die per wafer. If all 30 particles caused a defective die, the yield loss on the 600 die wafer would be only 5%, while that on the 300 die wafer would be 10%. Thus, the larger the die size the greater the effect of particles.

Electrostatically induced particles on the surface of the wafer can have adverse effects during the epitaxial growth process. These effects can be a deviation in the rate of formation of steps, the formation of imperfect nuclei, and dislocations in the crystal structure. It will be more pronounced for a given size of contaminant as device geometries shrink further.

Statically charged particles can also cause severe problems in gate oxidation steps in MOS and EPROM devices. Current technology is producing gate oxides only a few hundred angstroms thick. In the near future 50 angstroms thick oxides will be common. We have seen that any

charge on or near a wafer will attract and attach unwanted particles. It is obvious these particles can have detrimental effects on both device yield and long-term reliability. Since 50 angstrom particles are sufficient to cause gate oxide defects, the filtering of these particles is essential. Unfortunately, particles this small can pass through most filters and are below the detection threshold of most particle detectors. Therefore, even a Class 10 clean room may contain a high density of 50 to 100 angstrom particles.

Oxide is an amorphous form of glass consisting of a random network of silicon and oxygen atoms. Any particulate contaminant can disrupt this random structure such that crystalline regions will form. This crystalline structure is inherently more dense than the amorphous glass and the interface boundaries between them can be porous to impurities during subsequent processing steps. Devices with flawed gate oxides from particulate contaminants are also more susceptible to failure from electrical transients.

It should also be noted that besides being susceptible to defects from particulate contaminants, there are certain fabrication processes at which the devices are susceptible to damage from an ESD. Consider the following: in MOS wafer fabrication there is a step in which a thin layer of oxide is grown on the entire wafer surface on top of which is a layer of polysilicon which is later defined by photolithography and etched. Before the polysilicon is etched, it is in actuality forming a large capacitor between itself and the silicon substrate, providing the polysilicon is not in contact with the substrate. At this stage, the oxide is very susceptible to ESD due to its large contact area. However, once the polysilicon is defined to form the gate, source and drain, the capacitance is much reduced along with the possibility of damage.

Even though it was found (in Section 3.3) that the fabricated devices were very susceptible to ESD (even after glassivation), it should be noted that the post-fabricated device could be less

susceptible than the wafer at various points in its fabrication.

5.0 AIR IONIZATION

It is recognized that since normal ESD control techniques and equipment would be ineffective on the high static generative and insulative materials necessarily used during IC fabrication that air ionization is an effective means for controlling static levels. This section will present various methods of air ionization along with possible adverse effects.

Ionized air contains a high density of both positive and negative ions. If a surface develops a positive charge via triboelectrification, its electrostatic field will attract negative ions from the air and repel positive ions. As the negative ions collide with the positively charged surface, the surface is safely neutralized. When correctly applied, air ionizers provide a safe and effective method of preventing static charge build-up with existing equipment. An advantage of air ionizers is that few changes to work stations, carriers or clothing are required when they are used.

Additionally, ions in the air will also neutralize statically charged particles in the air. As we have seen before, a statically charged, nonconductive particle will stick to a neutralized surface nearly as well as a charged particle sticks to an oppositely charged surface. Wafer fabrication areas are particularly well-suited for air ionization because of the laminar air flow generally found in these clean rooms. The laminar air flow will rapidly distribute ions throughout the area without the use of extra fans.

Air ionizers come in three general types. Two are electrically generated, while the third uses a nuclear source.

Electrical ionizers are either AC or DC. The AC units are typically grids or strings of emitters connected to a central high-voltage AC power supply. Figure 5-1 shows an example of an AC ionizer.

These emitters alternately produce both positive and negative ions, positive during the positive voltage swing and negative during the negative voltage swing of each cycle.

DC ionizers are composed of pairs of emitters connected by low voltage (115V or 48V) wiring (Figure 5-2). Each pair contains one emitter which produces only positive ions and one emitter which produces only negative ions, since positive and negative ions tend to attract and neutralize each other. The separation of the positive and negative emitters in a DC ionizer gives the ions a much longer life and thus greater distribution throughout the area. However, objects near the negative emitter tend to develop a negative charge, while objects near the positive emitter tend to charge positively. A third alternative tries to get the best from both worlds. This is essentially a DC system with the positive and negative emitters placed in closely spaced (about six-inch separation) pairs. The positive and negative emitters are then alternately switched on and off at intervals of about 5 seconds. This provides a pulsed DC operation. This technique prevents the polarization noted in the straight DC units while employing the advantage of longer ion life.

Nuclear ionizers produce ions from the decay of low-level radioactive elements contained within the nuclear ionizer. Nuclear sources do not generally create as many ions as electronic units but do produce equal quantities of positive and negative ions from the same source. Thus the ion life is limited. However, the nuclear sources do not require power supplies; thus they require no wiring upon installation nor any maintenance. Unfortunately, they cannot be purchased (only leased) and must be replaced every year.

Electronic ionizers involve several potential dangers which prospective users should be aware of. While most of these problems have been overcome by the majority of electronic ionizer manufacturers, each ionizer should be carefully inspected and tested for these problems both at installation as well as periodically after installation.

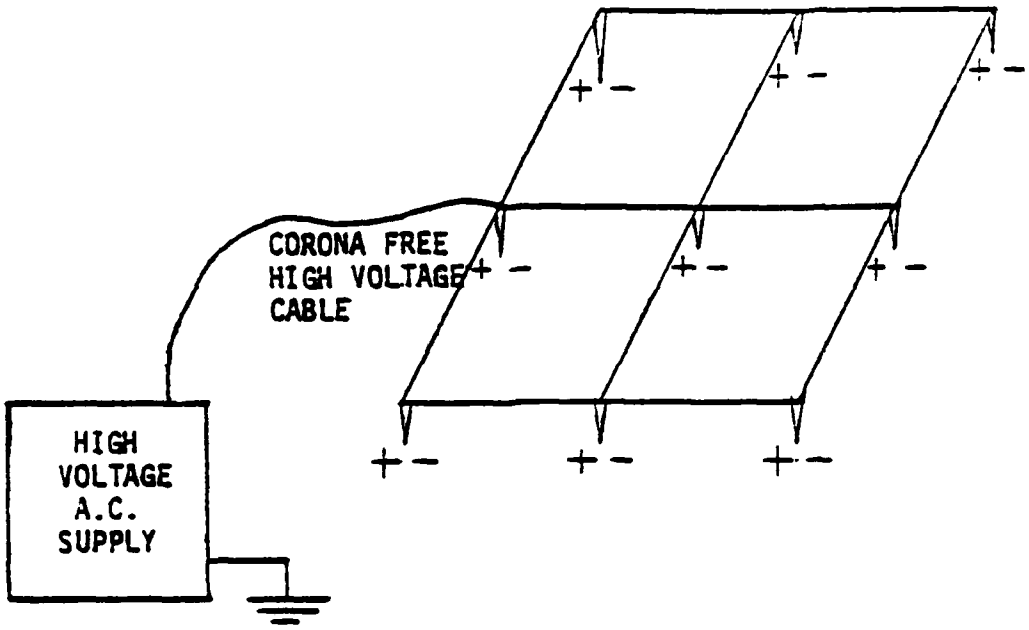


FIGURE 5-1: "GRID" TYPE AIR IONIZER
EMITTERS PRODUCE BOTH POSITIVE AND
NEGATIVE IONS

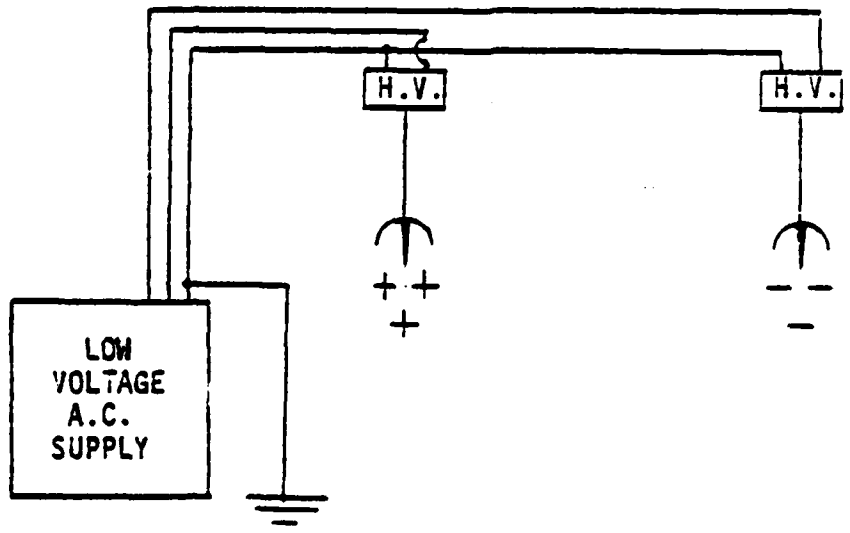


FIGURE 5-2: "BIPOLAR" TYPE AIR IONIZER
EACH EMITTER PRODUCES EITHER POSITIVE OR
NEGATIVE IONS.

Air ionizers do not prevent static generation; they can only neutralize a surface which has already been charged. The neutralization time, which varies for different materials, ionizer type, orientation, etc., can be sufficiently long to allow devices on the wafer to be damaged before the charge is neutralized. In this situation, the use of conductive materials is normally desirable; however, as we have seen their use is limited in an IC fabrication clean room.

Electrical air ionizers are generally cheaper and produce more ions than nuclear ionizers. However, they can develop side effects which may be very disastrous to a wafer fabrication line. Electrical ionizers if improperly designed or installed may generate small amount of ozone. Ozone will cause scumming of most negative photoresists. The level of ozone required to cause scumming is considerably less than the level which can be smelled or that can be detected by meters designed to test for the O.S.H.A. health hazard level. Therefore, all candidate electrical ionizers should be carefully tested for ozone production before installation. Exposing a few wafers to a sample ionizer is a simple first step. However, ozone production may also be affected by installation. If an ionizing needle is placed too close to a grounded conductor (within 4 inches), the electric field between these two points may be sufficient to cause excessive ozone production. Also, the high-voltage cable that connects some types of ionizers may be damaged by mounting hooks or staples. If a staple damages the dielectric around the high voltage cable, the electric field between the cable and the staple may be sufficient to break down the small amount of dielectric remaining around the cable and again produce ozone. Installation of high-voltage cable should be carefully inspected as this mechanism may take months to fully develop.

Electronic noise (EMI) is another possible problem. Again, most electronic ionizers do not produce detectable amounts of EMI; however, manufacturing flaws or improper installation may cause the generation of noise. This noise can upset sensitive electronic controls used through

the wafer manufacturing area. Internal arcing of high-voltage circuits or the location of a ground too close to a needle will produce this noise. Fortunately, EMI is easy to detect. A spectrum analyzer with a small antenna will serve well. A simple FM transistor radio will also detect most problems.

It should also be noted that EMI and ozone generation are often related. The corona discharge or arcing that produces ozone usually generates EMI. Thus, a simple EMI check can also guard against ozone contamination. A periodic EMI check is recommended in any electrically ionized wafer fabrication area.

Another problem which may be experienced with electronic ionizers is needle erosion. Needle erosion results from the constant impact of oppositely charged particles drawn toward the needle. Small particles can reach very high velocities when interacting with the strong electrical field from the needle. These particles impact the needle point with sufficient energy to dislodge soft material. Needles made of surgical steel do not exhibit this problem but needles made of softer material (Au or Ag plated) will erode within one year.

Nuclear ionizers are not subject to any of these problems. Installation is not critical and they do not require periodic checks. However, they must be leased and replaced annually and are effective over only a small area, making them inadequate for most clean room applications.

Although air ionization has been around for some time, it is evident that much work needs to be done for its use in clean room applications.

6.0 CONCLUSIONS

Static electricity may be very hazardous in a wafer fabrication facility. Static charges are inherently prevalent in a clean room and attract and hold airborne particles to wafers and masks. These particles can create defects during photolithography and oxidation, possibly making the device more susceptible to ESD damage and more prone to latent failures.

Devices in wafer form are also very susceptible to damage from ESD. There are many subtle susceptibility modes of devices in wafer form, and the input protection circuitry on the die are ineffective in preventing electrostatic discharge damage.

The damage caused by electrostatic discharge to a wafer often appears as missing or faulty geometries. This damage may be easily misidentified as a particle or photoresist problem; however, careful inspection will show damage to more than one layer if the defect was caused by ESD.

Photomasks are also susceptible to electrostatic discharge although photolithography defects affect only one layer.

Air ionization is an effective means of neutralizing static charges and will probably become necessary in fabrication facilities producing submicron device structures. However, more development work in air ionizers must be done, and care must be taken to avoid potentially disastrous side effects when they are used.

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